REMARKS

Claims 1-29 are pending in the application. Claim 1 is independent. No claims have been amended.

Restriction/Election Requirement

In the Office Action, the Examiner requested that Applicant affirm the election of Group 1, claims 1-4 made on November 9, 2004. Applicant hereby affirms the the election of Group 1, claims 1-4.

Rejection of Claims 1-4 Under 35 U.S.C. § 103(a)

In the Office Action, the Examiner rejected claims 1-4 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No.5,089,880 to Meyer et al. (hereinafter "Meyer") in view of U.S. Patent No.5,558,928 to DiStefano et al. (hereinafter "DiStefano"). To establish a *prima facie* case of obviousness, an Examiner must show three things: (1) that there is some suggestion or motivation to modify a reference or combine reference teachings to arrive at the claimed invention, (2) that there must be a reasonable expectation of success, and (3) that the references teach or suggest each and every element of the claimed invention. (MPEP §2143) Applicant respectfully traverses the rejection.

Embodiments of the present invention are directed to stacking of wafers, such as printed circuit boards made from a layer of bulk silicon 102 on the bottom, a layer of active silicon 104 on the bulk silicon 102, one or more metal interconnect levels 106 on the active silicon, and a top metal pattern 108 on the interconnect levels 106. (*See* Applicant's Specification at paragraph **[0014]**.) Claim 1 recites in pertinent part "a first wafer having a first metal pattern disposed on a top surface; a second wafer having a second metal pattern disposed on a top surface; and an interposer disposed between the top surface of the first wafer and the top surface of the second wafer, the interposer having a pattern of metal vias disposed in a cured thermosetting plastic, the pattern of

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metal vias being aligned with and electrically coupled to the first metal pattern and the second metal pattern" (emphasis added).

Meyer appears to be directed to stacking of individual layers to fabricate a printed circuit board. In Meyer, the printed circuit board has alternating ***signal planes and several ground planes*** (emphasis added). (Column 5, lines 34-35). Thus, Meyer does not appear to be directed to stacking multiple printed circuit boards, but planes within a single printed circuit board. Accordingly, Applicant respectfully submits that Meyer is not properly applied to the claimed invention.

DiStefano also appears to be directed to stacking of individual layers to fabricate a printed circuit board. For example, DiStefano provides at column 5, lines 38-41 that an interior element may incorporate an electrically conductive structure which serves to define a potential plane such as ***a ground plane in the finished assembly*** (emphasis added). Applicant respectfully submits therefore that DiStefano is not properly applied to the claimed invention either.

Applicant respectfully submits that because Meyer and DiStefano are not properly applied to the claimed invention that claims 1-4 are patentable over Meyer and DiStefano. Accordingly, Applicant respectfully requests that the Examiner reconsider and remove the rejection to claims 1-4.

CONCLUSION

Applicants submit that all grounds for rejection have been properly traversed and that the application is in condition for allowance. The Examiner is invited to telephone the undersigned representative if the Examiner believes that an interview might be useful for any reason.

Respectfully submitted,
BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN

Date: February 16, 2005

Jan Little-Washington
Reg. No.: 41,181

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Date of Deposit

Yuko Tanaka
Name of Person Mailing Correspondence

Y. Tanaka
Signature

February 16, 2005
Date